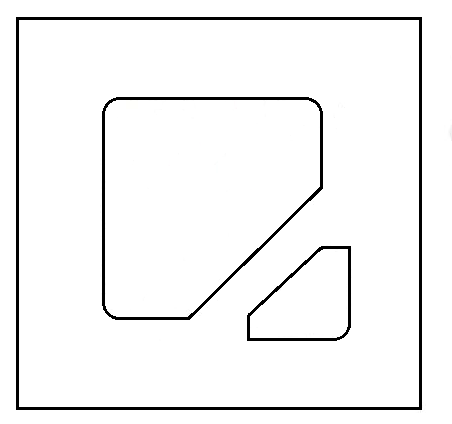
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.028”**



**A**

**C**

**.015”**

**.015”**

**.007”**

**.028”**

**BACKSIDE IS CATHODE AND IS COMMON TO TOP CATHODE PAD**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .007” min.**

**Backside: COMMON**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .028” X .028” DATE: 10/21/21**

**MFG: CDI THICKNESS .009” P/N: 1N823**

**DG 10.1.2**

#### Rev B, 7/19/02